management of different hardware events of a chip card while providing high security. Thus, the device according to the invention offers the possibility of detection when the user of an application tries to exceed his rights, for example, by attempting to access data not intended for the application in question.

To achieve this objective, the device sets up specific instructions internal to the microprocessor of the chip card. These specific instructions are call instructions and return instructions. These call and return instructions are associated with specific registers for determining whether the operations performed by the application are authorized.

The invention therefore pertains to a device for accessing applications of a chip card comprising a microprocessor associated with an operating system working with a set of instructions, a program memory, and one or more applications in a memory of the chip card.

The device comprises a register of the microprocessor to store a code on several check bits proper to an entity brought into play. Also included are a call instruction, and an instruction for the return of the set of instructions to instantaneously and automatically update the register during the action by a new entity. The device further includes a checking device for checking, as a function of the check bits, whether access to the zones or address location of the memory of the chip card by the new entity that is called or comes into action in the chip card is authorized. A first link transmits the check bits from the microprocessor to the checking device.

According to a particular embodiment of the device of the invention, each new entity being executed is activated at a predefined address of a read only

memory (ROM) of the chip card. According to different embodiments of the invention, the entity operating in the chip card may be an application of the one or more applications or a hardware event, or the operating system associated with the microprocessor of the chip card.

Brief Description of the Drawings

The various aspects and advantages of the invention shall appear more clearly hereinafter in the following description made with reference to the appended figures which are given purely by way of an indication and in no way restrict the scope of the invention, and which are now introduced:

FIG. 1 is a simplified block diagram of a software architecture for the chip cards currently being developed according to the prior art; and

Figure 2 is a block diagram illustrating the principle of operation for the execution of an application within a chip card according to the present invention. A microprocessor 200 manages the set of operations for a plurality of applications 210 of the chip card 100.

Detailed Description of the Preferred Embodiments

A two-way bus 250 exchanges information between the microprocessor 200 and any application of the plurality of applications 210-212. The information exchanged may be data elements, addresses or control instructions. An access controller to the memory 220 exchanges information with the microprocessor 200 using a link 230, which conveys a control signal between the microprocessor 200 and the controller providing access to the memory 220.

When an entity such as the application 211, for example, requires the intervention of another entity, such as an application 212, it sends a call instruction DCALL using the two-way bus 250 followed by a designation of the entity called and a parameter enabling the nature of the call to be determined. According to the invention, a register R is updated during such calls. A certain number of bits of the register R then assume a value associated with the called entity. The register R is therefore a hardware component of the microprocessor 200 used to store a code proper to the entity of the software architecture that is being performed, and to control its field of execution.

Furthermore, the device according to the invention may also take into account instructions known as hardware instructions, such as resetting type instructions, for example. Instructions known as hardware instructions are events that may occur in real time and generate interruptions in the microprocessor of the chip card. This type of event is managed by the device in the same way as the software instructions. The bits of the register R take a very precise value appropriate to each real-time event affecting the chip card, thus limiting and controlling the rights pertaining to these events.

The information given by the register R is thus capable of checking information on the identification of the zone of the software architecture concerned by the application being executed. This information is checked at the microprocessor or at any other entity external to the software architecture.

The information given by the register R enables the checking of the zone of the memory of the chip card in which the application is permitted to be